EE 434 Name _____
FINAL EXAM
Fall 2005

Instructions. You may bring up to 6 sheets of notes to this exam which is comprised of 8 problems and 10 questions. The weight for each question is 2 points and for each problem is 10 points. Please solve the problems and include your answers directly on the exam sheet.

Unless specified directly in a problem, if references to semiconductor processes are needed, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=30\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, Cbdbot = $0.5fF/\mu^2$, and Cbdsw = $2.5fF/\mu$. and all npn bipolar transistors are characterized by the parameters $\beta =100$, $V_{AF}=4$, and $J_S= 3E\text{-}19A/\mu^2$. If more detailed process parameters are needed, refer to the list of parameters on the last page of this exam. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Q1 What are the two reasons the fuses see minimal use in FPGAs?

Q2 How many transistors are needed for a clocked edge-triggered master-slave S-R flip flop if static CMOS gates are used to implement the entire structure?

Q3 There are two main strategies used to implement the Boolean Blocks in an FPGA. What are they?

Q4 Why is the turn-around for mask-programmable ROM arrays much quicker than for full-custom logic?

Q5 Pad drivers are widely used in conjunction with designing Boolean systems. What is the major purpose of pad drivers?

Q6 If you have a choice of building a variety of logic functions using either all Static CMOS NAND gates or all Static CMOS NOR gates and if all gates are to be sized for equal worst-case rise and fall times, will the NAND or the NOR style provide, on the average, lower static power dissipation? Why?

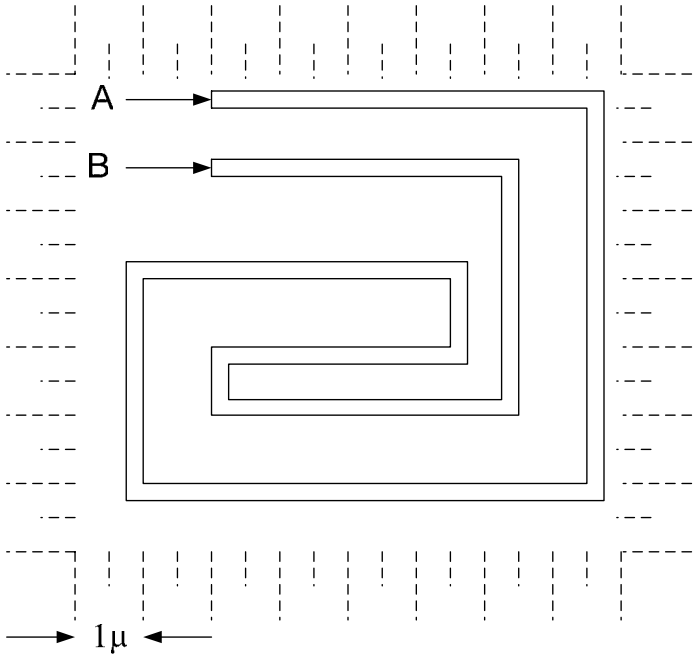
Q7 What is the major reason NMOS logic has been replaced with CMOS logic in large digital systems designed today?

Q8 What will be the approximate minimum gate length in semiconductor processes in the year 2010?

Q9 Why is the clock period of a microprocessor so much longer than the propagation delay of the basic gates that are internal to the processor?

Q10 What is the major reason contacts to poly are not allowed on top of the channel region of the MOS transistor?

Problem 1 The layout of a resistor in Poly 2 is shown. Determine the resistance between nodes A and B. The width of the resistor body is 0.25μ. A grid surrounding the resistor has spacing between the major grid marks as indicated.

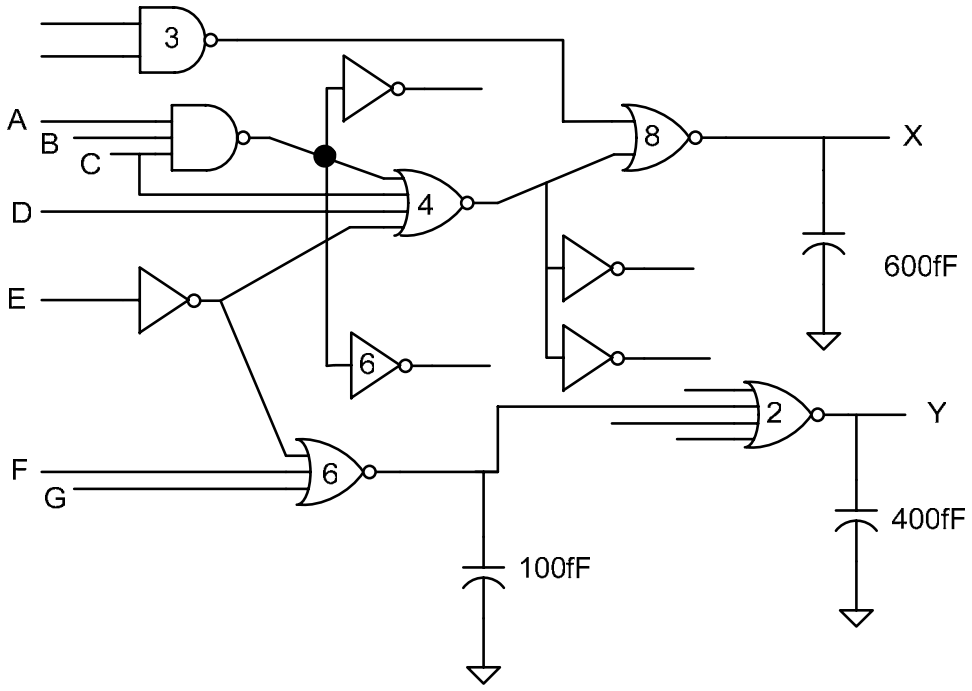


Problem 2 Assume the cost of 8 inch wafers in a 0.25µ process is $1200, the cost of 12 in wafers in a 0.1µ process is $3600, the defect density in the 0.25µ process is 1.5/cm^2 and the defect density in the 0.1µ process is 0.75/cm^2. If the cost per good die of an all-digital circuit in the 0.25µ process is $0.40, what would be the anticipated manufacturing cost of the same circuit in the 0.1µ process?

Problem 3 A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 2fF and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the E input to the Y output

b) Repeat part a) if the 4-input NOR gate uses all minimum sized transistors.

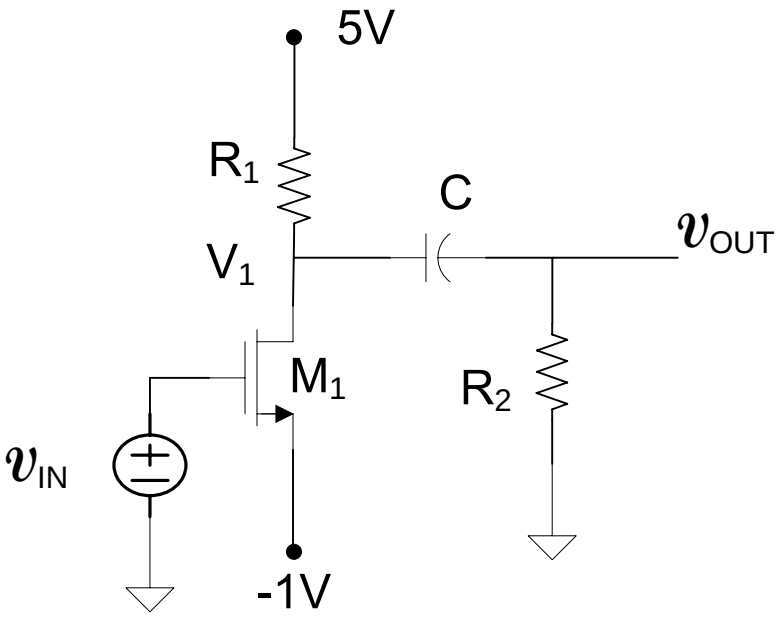


Problem 4 Assume that amplifier shown is to be fabricated in a 0.5μ process with process parameters determined on the last page of this exam. The resistor R_1 is 10KΩ, R_2 is 5KΩ and the capacitor C is large.

a) If the drawn length of the transistor is 0.6μ, determine the width so that the quiescent value of the voltage V_1 is 2V.

b) With the device sized as specified in part a), determine $v_{OUT}(t)$ if

$v_{IN}(t)=.001\sin 500t$.

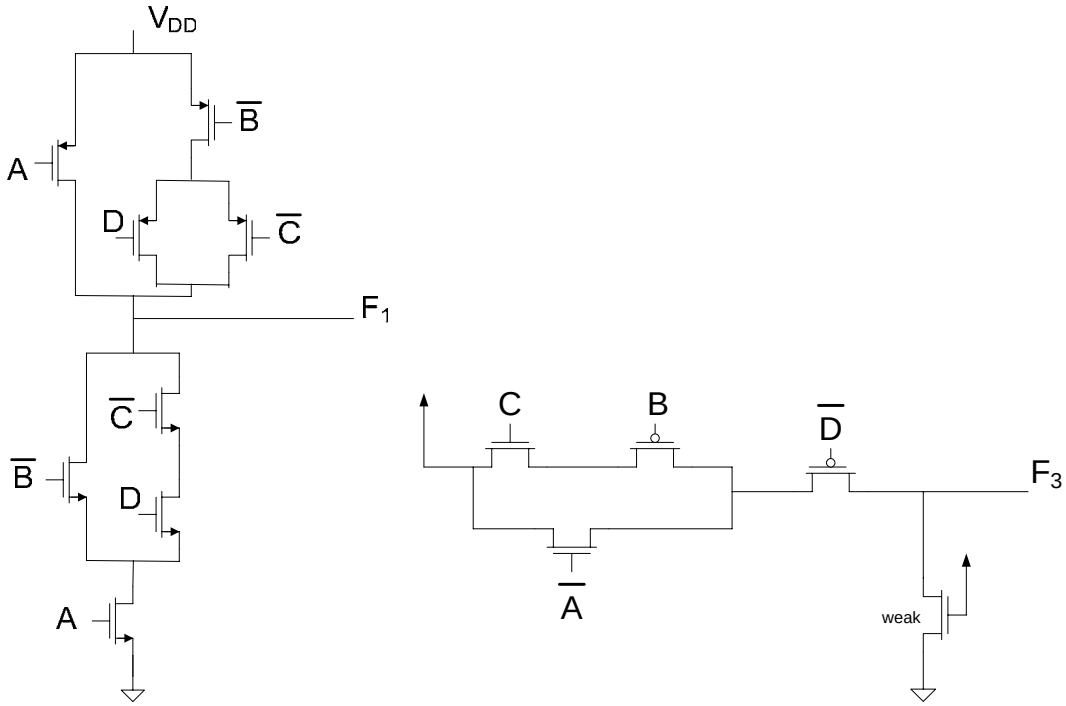


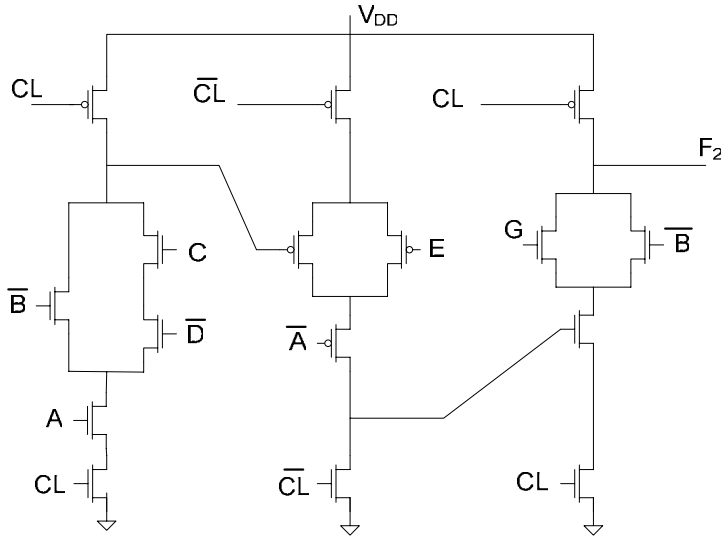
Problem 5 A signal X appears at the input of a minimum-sized equal rise/fall time inverter. This signal must be taken off-chip. The total capacitance seen at the pad for taking this signal off chip is 40pF.

a) What is the size of the n-channel transistor in the last stage of an equal rise/equal fall pad driver that is designed to minimize the delay in driving the load. Assume you are working in a 0.5μ CMOS process

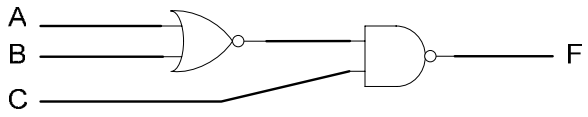
b) What is the dynamic power dissipation in the last stage of this pad driver?

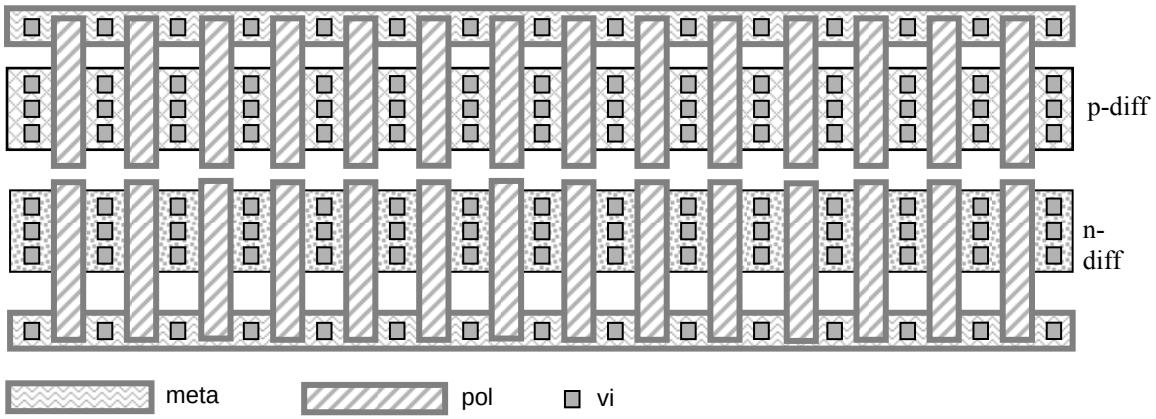
Probhlem 6 Three logic circuits are shown. For each circuit, identify the type of logic that is being used and determine the corresponding output variable F.





Problem 7 A sea of gates array is shown. With metal interconnect and appropriate vias, program this array to implement the function indicated by the circuit shown. Show where V_{DD} and V_{SS} are connected to the array as well.

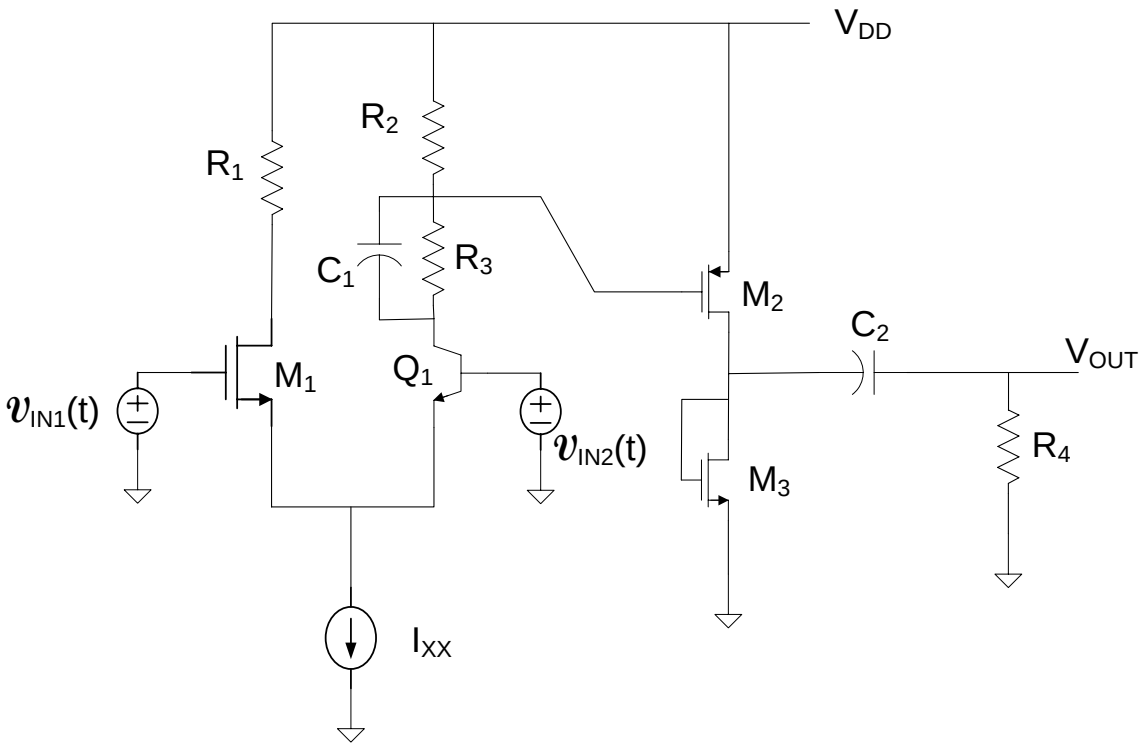




Problem 8 Assume all capacitors are large and that the MOS transistors are operating in the saturation region and that the BJT is operating in the forward active region.

a) Draw the dc equivalent circuit for this amplifier.

b) Draw the small-signal equivalent circuit using the dependent-source models for the active devices. You may neglect the output conductance in the small-signal models for all devices.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um